UNITED STATES DISTRICT COURT

Art Unit: 2836

Amendment filed June 21, 2004

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Amendments to the Claims

1. (Currently Amended) An electrostatic discharge (ESD) protection circuit comprising:

an NMOS transistor connected between an input/output pad and a ground, the NMOS transistor having a parasitic bipolar transistor; and

at least one diode among a plurality of N diodes, connected between the input/output pad and the NMOS transistor, a cathode of said at least one diode being connected to the ground,

wherein, p+ and n+ junctions of a first diode of the plurality of N diodes are connected to the input/output pad and a p+ junction of a second diode of the plurality of N diodes, respectively,

the second diode through the N-1 diode of the plurality of N diodes are connected such that an n+ junction of each of the second diode through the N-1 diode is connected to the p+ junction of a subsequent diode, and an n+ junction of an N diode is connected to the substrate.

2. (Currently Amended) The ESD protection circuit of claim 1, wherein an output terminal of the at least one diode among a plurality of N the diodes is connected to a base of the parasitic bipolar transistor.

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3. (Currently Amended) The ESD protection circuit of claim 1, wherein the said at least one diode is a PN diode.

(Canceled) 4.

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(Currently Amended) The ESD protection circuit of claim 1, wherein the at least one diode includes a plurality of N diodes, and

a count of the diodes N of the plurality of N diodes is determined so as to stop a current flow through the at least one diode during a normal operation of a chip.

6. (Currently Amended) The ESD protection circuit of claim 1[[4]], wherein, the plurality of N diodes are connected in series to each other in a forward direction.

7. (Canceled)

(Currently Amended) An electrostatic discharge (ESD) protection circuit comprising:

an input/output pad;

a plurality of N diodes connected in series between the input/output pad and a substrate of an NMOS transistor; and